**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

Claim 1 (currently amended): A phase detector, comprising:

a first input that receives a reference clock signal;

a second input that receives a comparison signal; and

a comparison circuit that receives the reference clock signal and compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

Claim 2 (original): The phase detector of claim 1, wherein the comparison circuit comprises:

a first circuit that asserts a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

a second circuit that asserts a second signal having the predetermined logic level in response to either one of a leading edge and a trailing edge of the comparison signal.

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Claim 3 (original): The phase detector of claim 2, wherein the comparison circuit further comprises:

a reset circuit that generates a reset signal that resets both the first circuit and the second circuit in response to both the first signal and the second signal being asserted.

Claim 4 (original): The phase detector of claim 3, wherein the reset circuit comprises a delay circuit that delays generation of the reset signal for a predetermined length of time after both the first signal and the second signal are asserted.

Claim 5 (original): The phase detector of claim 2, wherein the second circuit is a dual-edge triggered latch.

Claim 6 (original): The phase detector of claim 5, wherein the dual-edge triggered latch comprises:

a first latch device coupled to receive the comparison signal in a way such that the first latch device generates a first latch output signal having a predetermined logic level in response to a leading edge of the comparison signal;

a second latch device coupled to receive the comparison signal in a way such that the second latch device generates a second latch output signal having the predetermined logic level in response to a trailing edge of the comparison signal; and

a combining logic circuit that generates the second signal by combining the first latch output signal and the second latch output signal.

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Claim 7 (original): The phase detector of claim 6, wherein the combining logic circuit is a logical OR gate.

Claim 8 (original): The phase detector of claim 6, wherein the dual-edge triggered latch further comprises:

a reset input for receiving a reset signal that resets both the first latch device and the second latch device.

Claim 9 (canceled)

Claim 10 (previously presented): The phase-locked loop of claim 13, wherein the circuit that generates the comparison signal is a latch device configured to toggle a latch device output state once for each cycle of the divided frequency signal.

Claim 11 (original): The phase-locked loop of claim 10, wherein the latch device is configured to toggle the latch device output state once for each leading edge of the divided frequency signal.

Claim 12 (original): The phase-locked loop of claim 10, wherein the latch device is configured to toggle the latch device output state once for each trailing edge of the divided frequency signal.

Claim 13 (previously presented): A phase-locked loop comprising:

a phase detector that has a reference signal input that receives a reference clock signal and a comparison signal input that receives a comparison signal, wherein the phase detector generates a phase difference signal that represents a phase difference between the reference signal and a signal having twice the frequency of the comparison signal;

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a circuit that generates a phase-locked loop output signal having a frequency that is a function of the phase difference signal;

a frequency divider that receives the phase-locked loop output signal and generates therefrom a divided frequency signal; and

a circuit that generates the comparison signal from the divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal, wherein the phase detector comprises:

a comparison circuit that compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

Claim 14 (original): The phase detector of claim 13, wherein the comparison circuit comprises:

a first circuit that asserts a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

a second circuit that asserts a second signal having the predetermined logic level in response to either one of a leading edge and trailing edge of the comparison signal.

Claim 15 (original): The phase detector of claim 14, wherein the comparison circuit further comprises:

a reset circuit that generates a reset signal that resets both the first circuit and the second circuit in response to both the first signal and the second signal being asserted.

Claim 16 (original): The phase detector of claim 15, wherein the reset circuit comprises a delay circuit that delays generation of the reset signal for a predetermined length of time after both the first signal and the second signal are asserted.

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Claim 17 (original): The phase detector of claim 14, wherein the second circuit is a dual-edge triggered latch.

Claim 18 (original): The phase detector of claim 17, wherein the dual-edge triggered latch comprises:

a first latch device coupled to receive the comparison signal in a way such that the first latch device generates a first latch output signal having a predetermined logic level in response to a leading edge of the comparison signal;

a second latch device coupled to receive the comparison signal in a way such that the second latch device generates a second latch output signal having the predetermined logic level in response to a trailing edge of the comparison signal; and

a combining logic circuit that generates the second signal by combining the first latch output signal and the second latch output signal.

Claim 19 (original): The phase detector of claim 18, wherein the combining logic circuit is a logical OR gate.

Claim 20 (original): The phase detector of claim 18, wherein the dual-edge triggered latch further comprises:

a reset input for receiving a reset signal that resets both the first latch device and the second latch device.

Claim 21 (currently amended): A method of generating a phase difference signal, comprising:

receiving a reference clock signal;

receiving a comparison signal; and

generating the phase difference signal by directly comparing a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

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Claim 22 (original): The method of claim 21, wherein generating the phase difference signal comprises:

asserting a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

asserting a second signal having the predetermined logic level in response to either one of a leading edge and a trailing edge of the comparison signal.

Claim 23 (original): The method of claim 22, wherein generating the phase difference signal further comprises:

de-asserting both the first signal and the second signal in response to both the first signal and the second signal being asserted.

Claim 24 (original): The method of claim 23, wherein de-asserting both the first signal and the second signal comprises delaying de-assertion of the first signal and the second

signal for a predetermined length of time after both the first signal and the second signal are asserted.

Claim 25 (canceled)

Claim 26 (previously presented): The method of claim 29, wherein generating the comparison signal comprises toggling a latch device output state once for each cycle of the divided frequency signal.

Claim 27 (original): The method of claim 26, wherein generating the comparison signal comprises toggling the latch device output state once for each leading edge of the divided frequency signal.

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Claim 28 (original): The method of claim 26, wherein generating the comparison signal comprises toggling the latch device output state once for each trailing edge of the divided frequency signal.

Claim 29 (previously presented): A method of generating a phase-locked loop output signal, comprising:

generating a phase difference signal that represents a phase difference between a reference clock signal and a signal having twice the frequency of a comparison signal by comparing a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal;

generating the phase-locked loop output signal having a frequency that is a function of the phase difference signal;

receiving the phase-locked loop output signal and generating therefrom a divided frequency signal; and

generating the comparison signal from the divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal.

Claim 30 (original): The method of claim 29, wherein comparing the phase of the reference clock signal with the phase of the signal having the frequency that is twice that of the comparison signal comprises:

asserting a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

asserting a second signal having the predetermined logic level in response to either one of a leading edge and trailing edge of the comparison signal.

Claim 31 (original): The method of claim 30, wherein comparing the phase of the reference clock signal with the phase of the signal having the frequency that is twice that of the comparison signal further comprises:

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generating a reset signal that de-asserts both the first signal and the second signal in response to both the first signal and the second signal being asserted.

Claim 32 (original): The method of claim 31, wherein generating the reset signal comprises delaying generation of the reset signal for a predetermined length of time after both the first signal and the second signal are asserted.

Claim 33 (previously presented): A phase-locked loop comprising:

a phase detector that has a reference signal input that receives a reference clock signal and a comparison signal input that receives a comparison signal, wherein the phase detector generates a phase difference signal that represents a phase difference between the reference signal and a signal generated by the phase detector having twice the frequency of the comparison signal;

a circuit that generates a phase-locked loop output signal having a frequency that is a function of the phase difference signal;

a frequency divider that receives the phase-locked loop output signal and generates therefrom a divided frequency signal; and

a circuit that generates the comparison signal from the divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal.

Claim 34 (previously presented): The phase-locked loop of claim 33, wherein the circuit that generates the comparison signal is a latch device configured to toggle a latch device output state once for each cycle of the divided frequency signal.

Claim 35 (previously presented): The phase-locked loop of claim 34, wherein the latch device is configured to toggle the latch device output state once for each leading edge of the divided frequency signal.

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Claim 36 (previously presented): The phase-locked loop of claim 34, wherein the latch device is configured to toggle the latch device output state once for each trailing edge of the divided frequency signal.

Claim 37 (previously presented): A method of generating a phase-locked loop output signal, comprising:

generating a phase difference signal from a reference clock signal and a signal having twice the frequency of a comparison signal;

generating the phase-locked loop output signal having a frequency that is a function of the phase difference signal;

receiving the phase-locked loop output signal and generating therefrom a divided frequency signal; and

generating the comparison signal from the divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal.

Claim 38 (previously presented): The method of claim 37, wherein generating the comparison signal comprises toggling a latch device output state once for each cycle of the divided frequency signal.

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Claim 39 (previously presented): The method of claim 38, wherein generating the comparison signal comprises toggling the latch device output state once for each leading edge of the divided frequency signal.

Claim 40 (previously presented): The method of claim 38, wherein generating the comparison signal comprises toggling the latch device output state once for each trailing edge of the divided frequency signal.